FABRICATION METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a fabrication technique of a semiconductor integrated circuit device, particularly to a technique effective when applied to a wafer-level electrical test of a semiconductor integrated circuit device.

Probe test is one of the techniques employed for the inspection of semiconductor integrated circuit devices. It includes a function test for confirming whether a wafer functions to specification or not, or a test for judging whether the wafer is non-defective or defective by measuring its DC operating characteristics and AC operating characteristics.

In recent years, a probe test of semiconductor integrated circuit devices tends to be carried out while they are in the stage of a semiconductor wafer (which will hereinafter be called "wafer" simply) to satisfy the request for shipment in the wafer form (differentiation of products), KGD (Known Good Die) (improvement in the yield of MCP (Multi-Chip Package)) and reduction in the total cost.

Disclosed, for example, is a prober used for a wafer-level probe test which comprises a multilayer film having a plurality of contact terminals disposed in a predetermined region on the probing side, a lead-out wire to be electrically connected to each contact terminal and a ground layer opposite

to the lead-out wire with an insulating layer sandwiched therebetween and is attached to a holding member to eliminate the slack of the region. Further, this prober has a constitution in which a specific compliance mechanism is engaged with the holding member while applying a contact pressure thereto by a contact pressure applying unit (for example, refer to Patent Documents 1 and 2).

As a unit for forming the contact terminals and lead-out wires, disclosed is a technique of forming molds for the formation of the contact terminals by anisotropic etching of a silicon wafer, forming the contact terminals and lead-out wires by using the molds, and then removing the silicon wafer molds after the formation of the contact terminals and lead-out wires (for example, refer to Patent Documents 3 and 4).

Patent Document 1: Japanese Patent Application Laid-Open No. Hei 11(1999)-23615

Patent Document 2: Japanese Patent Application Laid-Open No. Hei 10(1998)-308423

Patent Document 3: Japanese Patent Application Laid-Open No. Hei 11(1999)-97471

Patent Document 4: Japanese Patent Application Laid-Open No. Hei 7(1995)-283280

SUMMARY OF THE INVENTION

With capacity expansion of memory products and increase in the production amount of logic products with a built-in

memory, each a type of semiconductor integrated circuit devices, time required for a wafer-level probe test is on increase. There is therefore a demand for improvement in the throughput of the wafer-level probe test. In order to improve this throughput, it is necessary to reduce the time spent for the test per wafer. The time T0 required for the test per wafer is represented by the equation: $T0=(T1+T2)\times N+T3$, wherein T1 is time necessary for a single test by a prober, T2 is time necessary for indexing of a prober, N is the number of times to bring a probe (probe needle) of the prober into contact with the wafer (which will hereinafter be called "touchdown times"), and T3 is time necessary for replacement of the wafer with a new one. According to this equation, the number of touchdown times must be reduced in order to improve the throughput of the wafer-level probe test.

For a reduction in the fabrication cost of a semiconductor integrated circuit device, miniaturization of semiconductor elements and interconnects to narrow the area of a semiconductor chip (which will hereinafter be called "chip" simply) and thereby increase the number of chips obtained from one wafer has been pursued. Such a tendency accelerates narrowing of the pitch between test pads (bonding pads) and also decrease in their area. When the test is carried out using a prober having a cantilever type probe, the probe is wiped on the surface of a test pad in order to break a natural oxide film formed on the surface of the test pad and bring the

probe into contact with the test pad. By this wiping of the probe, however, not only the natural oxide film is broken but also scratches appear on the surface of the test pad itself by the wiping. In consideration of a decreasing tendency of the test pad area as described above, a ratio of such scratches in the surface of the test pad shows a relative increase, leading to a problem that the adhesive force of a bonding wire connected to the test pad in the later step will lower.

An object of the present invention is to provide a technique capable of improving the throughput of an electrical test of a semiconductor integrated circuit in the wafer form.

Another object of the present invention is to provide a technique capable of reducing damages caused in a test pad upon testing of a semiconductor integrated circuit device.

The above-described and the other objects and novel features of the present invention will be apparent from the description herein and accompanying drawings.

Of the inventions disclosed in the present application, typical ones will next be summarized briefly.

In one aspect of the present invention, there is thus provided a fabrication method of a semiconductor integrated circuit device, comprising the steps of preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface, a plurality of first electrodes to be electrically connected

with the semiconductor integrated circuit; preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the plurality of first electrodes and interconnects to be electrically connected with the plurality of contact terminals, so as to cause the tip portions of the plurality of contact terminals to protrude toward the main surface of the semiconductor wafer; and bringing the plurality of contact terminals into contact with the plurality of first electrodes to perform an electrical test of the semiconductor integrated circuit device,

wherein, the tip portions of the plurality of contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

the first card has a plurality of connection mechanisms to be electrically connected to the plurality of second electrodes and pushing mechanisms for pushing the plurality of contact terminals toward the plurality of first electrodes,

the connection mechanisms each comprises an elastic contact needle for pushing the second electrodes by a load generated upon contact of the plurality of contact terminals with the plurality of first electrodes, and a retainer member for retaining the contact needle and is disposed to get in

touch with the second electrodes over the second surface of the first sheet,

each of the pushing mechanisms is formed by successively stacking a first elastic material, a pushing member and a second elastic material one after another from the side of the first sheet and is disposed above the plurality of contact terminals over the second surface of the first sheet, and

any one of the pushing mechanisms pushes at least one of the contact terminals.

In another aspect of the present invention, there is also provided a fabrication method of a semiconductor integrated circuit device, comprising the steps of preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface, a plurality of first electrodes to be electrically connected with the semiconductor integrated circuit; preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the plurality of first electrodes and interconnects to be electrically connected with the plurality of contact terminals, so as to cause the tip portions of the plurality of contact terminals to protrude toward the main surface of the semiconductor wafer; and bringing the plurality of contact terminals into contact with the plurality of first electrodes to perform an electrical test of the semiconductor integrated

circuit device,

wherein, the tip portions of the plurality of contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

the first card has a plurality of connection mechanisms to be electrically connected to the plurality of second electrodes,

the connection mechanisms each comprises an elastic contact needle for pushing the second electrodes by a load generated upon contact of the plurality of contact terminals with the plurality of first electrodes, and a retainer member for retaining the contact needle and is disposed to get in touch with the second electrodes over the second surface of the first sheet, and

the probe needle pushes the second electrodes before the plurality of contact terminals are brought into contact with the plurality of first electrodes.

In a further aspect of the present invention, there is also provided a fabrication method of a semiconductor integrated circuit device, comprising the steps of preparing a semiconductor wafer which has been divided into a plurality chip regions each having a semiconductor integrated circuit formed thereover, and has, formed over the main surface, a

plurality of first electrodes to be electrically connected with the semiconductor integrated circuit; preparing a first card for retaining a first sheet, which has a plurality of contact terminals to be brought into contact with the plurality of first electrodes and interconnects to be electrically connected with the plurality of contact terminals, so as to cause the tip portions of the plurality of contact terminals to protrude toward the main surface of the semiconductor wafer; and bringing the plurality of contact terminals into contact with the plurality of first electrodes to perform an electrical test of the semiconductor integrated circuit device;

wherein, the tip portions of the plurality of contact terminals are disposed over a first surface of the first sheet, and a plurality of second electrodes to be electrically connected with the interconnects are disposed over a second surface which is opposite to the first surface of the first sheet,

the first card has a plurality of connection mechanisms to be electrically connected to the plurality of second electrodes,

the connection mechanisms each comprises an elastic contact needle for pushing the surface of the second electrodes by a load generated upon contact of the plurality of contact terminals with the plurality of first electrodes, and a retainer member for retaining the contact needle and is

disposed to get in touch with the second electrodes over the second surface of the first sheet, and

the surface of each of the plurality of second electrodes to be brought into contact with the contact needle has been planarized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a fragmentary perspective view of a probe card according to one embodiment of the present invention;

FIG. 2 is a fragmentary perspective view of the upper surface of the probe card according to the one embodiment of the present invention;

FIG. 3 is a perspective view illustrating the constitution of a lower pushing unit included in the probe card according to the one embodiment of the present invention;

FIG. 4 is a fragmentary cross-sectional view of the lower pushing unit illustrated in FIG. 3;

FIG. 5 is a plan view of a thin film probe included in the lower pushing unit illustrated in FIG. 3;

FIG. 6 is a fragmentary enlarged plan view of the thin film probe illustrated in FIG. 5;

FIG. 7 is a plan view of a thin film probe included in the lower pushing unit illustrated in FIG. 3;

FIG. 8 is a fragmentary enlarged plan view of the thin film probe illustrated in FIG. 7;

FIG. 9 is a fragmentary cross-sectional view for

illustrating the fabrication step of the thin film probe described based on FIGS. 4 to 8;

FIG. 10 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 9;

FIG. 11 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 10;

FIG. 12 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 11;

FIG. 13 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 12;

FIG. 14 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 13;

FIG. 15 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 14;

FIG. 16 is a fragmentary cross-sectional view of the thin film probe during a manufacturing step following the step of FIG. 15;

FIG. 17 is a plan view illustrating one example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 18 is a plan view illustrating another example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 19 is a plan view illustrating a further example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 20 is a plan view illustrating a still further example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 21 is a plan view illustrating a still further example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 22 is a plan view illustrating a still further example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 23 is a plan view illustrating a still further example of the arrangement of chip regions, in the wafer plane, to be tested by a semiconductor prober by single contact of a probe card;

FIG. 24 is a plan view illustrating a still further example of the arrangement of chip regions, in the wafer plane,

to be tested by a semiconductor prober by single contact of a probe card;

FIG. 25 is a flow chart illustrating the fabrication steps of the semiconductor integrated circuit device according to the one embodiment of the present invention;

FIG. 26 is a perspective view illustrating the constitution of a lower pushing unit included in a probe card according to another embodiment of the present invention;

FIG. 27 is a fragmentary cross-sectional view of a lower pushing unit included in a probe card according to a further embodiment of the present invention; and

FIG. 28 is a fragmentary cross-sectional view illustrating one example of a POGO pin.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to the detailed description of the present application, the meanings of the terms used herein will next be described.

The term "wafer" means a single crystal silicon substrate (usually having a substantially circular plane), an SOI (Silicon On Insulator) substrate, a sapphire substrate, a glass substrate, or any other insulating, semi-insulating or semiconductor substrate, or a composite substrate thereof which is used for the fabrication of integrated circuits. The term "semiconductor integrated circuit device" as used herein means not only those fabricated on a semiconductor or

insulator substrate such as silicon wafer or sapphire substrate but also those formed over other insulating substrates such as glass substrates, e.g., TFT (Thin Film Transistor) and STN (Super-Twisted-Nematic) liquid crystals, unless otherwise specifically indicated.

The term "device surface" means a main surface of a wafer on which device patterns corresponding to plural chip regions are formed by lithography.

The term "contact mechanism" means a silicon wafer integrally formed with interconnect layers and contact terminals having a tip portion connected therewith by employing a wafer process similar to that used for the fabrication of a semiconductor integrated circuit, that is, a patterning method using photolithography, CVD (Chemical Vapor Deposition), sputtering and etching in any combination.

The term "thin film probe" means a thin film which has, disposed thereover, contact terminals to come in contact with a wafer to be tested, and interconnects which are led from the contact terminals and have an electrode for outside contact. The thickness of this thin film is about 10 μm to 100 μm.

The term "POGO pin" means a contact needle to be electrically connected with an electrode (terminal) by pressing a contact pin (plunger (contact needle)) against the electrode by making use of an elastic power of a spring (coil spring). It has, for example, a constitution as illustrated in FIG. 28 in which a spring SPR disposed in a tube (retainer

member) TUB made of a metal transmits an elastic power to a contact pin PLG via a metal ball MBL.

The term "probe card" means a structural body having a contact terminal to be brought into contact with a wafer to be tested and a multilayer wiring substrate, while the term "semiconductor prober" means a prober having a probe card and a sample holder on which a wafer to be tested is placed.

The term "probe testing" means electrical testing of a semiconductor integrated circuit by pressing the tip portion of the contact terminal against an electrode formed over the main surface of a chip region for judging whether the circuit is defective or non-defective based on the results of a function test for finding whether the product functions to specification or tests of DC operating characteristics and AC operating characteristics.

The term "burn-in test" means a test of applying temperature and voltage stresses on chips for screening the chips which may be defective in future.

The term "simultaneous testing of multiple chip regions" means simultaneous electrical testing of a plurality of chip regions of a semiconductor integrated circuit. The term "simultaneous testing of super multiple chip regions" means simultaneous electrical testing of at least 64 chip regions (at least about 1000 pins) of a semiconductor integrated circuit.

The term "KGD (Known Good Die)" means a chip guaranteed

as non-defective among chips to be mounted in a bare chip form such as those in flip chip bonding. The term "chips guaranteed as non-defective" means that they have already been screened by a similar test to that employed for packaged products.

The term "index time" means a time from the completion of the test of one chip or wafer until a new chip or wafer is positioned and becomes ready for the test when chips or wafers are tested one by one.

In the below-described embodiments, a description will be made after divided in plural sections or in plural embodiments if necessary for convenience's sake. These plural sections or embodiments are not independent each other, but in a relation such that one is a modification example, details or complementary description of a part or whole of the other one unless otherwise specifically indicated.

In the below-described embodiments, when a reference is made to the number of elements (including the number, value, amount and range), the number is not limited to a specific number but can be greater than or less than the specific number unless otherwise specifically indicated or principally apparent that the number is limited to the specific number.

Moreover in the below-described embodiments, it is needless to say that the constituting elements (including element steps) are not always essential unless otherwise specifically indicated or principally apparent that they are essential.

Similarly, in the below-described embodiments, when a reference is made to the shape or positional relationship of the constituting elements, that substantially analogous or similar to it is also embraced unless otherwise specifically indicated or principally apparent that it is not. This also applies to the above-described value and range.

In all the drawings for describing the embodiments, like members of a function will be identified by like reference numerals and overlapping descriptions will be omitted.

In the drawings used in the below-described embodiments, even a plan view is sometimes partially hatched for facilitating understanding of it.

In the below-described embodiments, MISFET (Metal Insulator Semiconductor Field Effect Transistor) typifying field effect transistors will be abbreviated as MIS.

The embodiments of the present invention will hereinafter be described specifically based on drawings.

(Embodiment 1)

FIG. 1 is a fragmentary perspective view illustrating a probe card (first card) of Embodiment 1 from an upper angle.

The probe card of Embodiment 1 is formed, for example, by attaching an upper pushing unit and a lower pushing unit on a multilayer wiring substrate 1. As illustrated in FIG. 1, the upper pushing unit attached onto the upper surface of the multilayer wiring substrate 1 comprises a base holder 2, a pin 3, a linear push 4, a spring plunger 5, a lid 6, an adjust

holder 7, a bolt 8, a shim ring 9, an adjust bolt 10 and the like.

The base holder 2 receives a load applied to the probe card when it is brought into contact with a wafer to be tested and prevents the probe card from being distorted by the load. This structure makes it possible to avoid occurrence of a relative positional shift between a contact terminal of the probe card and an electrode (test pad (first electrode)) on the main surface of the wafer with which the contact terminal gets in touch. The relative position between the contact terminal and electrode will be described later.

The pin 3 is installed between the multilayer wiring substrate 1 and base holder 2 and determines the position of the base holder 2 on the multilayer wiring substrate 1.

The linear push 4 has a function of guiding, in the base holder 2, the adjust bolt 10 which extends from the upper pushing unit towards the lower pushing unit which will be described later and is disposed so as to maintain a space for the vertical movement of the adjust bolt 10.

The spring plunger 5 is attached to the base holder 2 from the side surface thereof and serves to control the position of the adjust bolt 10 in a horizontal direction relative to the upper surface of the multilayer wiring substrate 1 (which direction will hereinafter be called "XY direction").

The lid 6 serves to prevent the linear push 4, which has

been disposed in a hole formed in the base holder 2, from protruding over the base holder 2.

The shim ring 9 controls the space between the adjust bolt 10 and adjust holder 7.

The adjust bolt 10 reaches the lower pushing unit, which will be described later, through the upper pushing unit and multilayer wiring substrate 1 and controls the position, by rotation, in the height direction of the lower pushing unit. When the adjust bolt 10 is fixed, the upper pushing unit, multilayer wiring substrate 1 and lower pushing unit are integrated. After the completion of the adjustment of the position by the adjust bolt 10 in the height direction of the lower pushing unit, the adjust bolt 10 is fastened by the adjust holder 7 and bolt 8 to prevent the adjust bolt 10 from rotating and being disposed at a wrong position in the height direction of the lower pushing unit.

FIG. 2 is a fragmentary perspective view illustrating the fragment of the upper surface of the multilayer wiring substrate 1 to which the upper pushing unit has been attached.

As illustrated in FIG. 2, a number of wires 11 electrically connected to a contact terminal which the below-described lower pushing unit has are pulled out from the base holder 2, and they are electrically connected to a circuit formed over the multilayer wiring substrate 1 by being connected to respective connecting terminals over the upper surface of the multilayer wiring substrate 1.

FIG. 3 is a perspective view illustrating the constitution of the lower pushing unit to be attached to the lower surface of the multilayer wiring substrate 1.

As illustrated in FIG. 3, the lower pushing unit comprises POGO pins (connection mechanism) 12, supporting pin plate 13, POGO pin seating plates 14,15, pin 16, elastomer (second elastic material) 17, pusher (pushing member) 18, retainer plate 19, thin film probe (first sheet) 20, stretch holder 21, silicon rubber 22 and the like.

The POGO pins 12 are disposed in the number necessary for simultaneous testing of multiple chip regions or simultaneous testing of super multiple chip regions. Each of the POGO pins 12 is, at the lower end thereof, in contact with the thin film probe 20 and, at the upper end thereof, electrically connected to the wires 11 (refer to FIG. 2).

The POGO pin seating plates 14,15 having the POGO pins disposed thereon are used for the alignment of the POGO pins 12 in the XY direction and they are fixed to the base holder 2 (refer to FIG. 1) by the pin 16 and pin 3 (refer to FIG. 1), whereby the relative position to the base holder 2 in the XY direction is determined.

The stretch holder 21 holds the thin film probe 20 by attaching the film to the holder and keeps the correct position of the thin film probe 20 in the XY direction and height direction with high accuracy.

The pusher 18 is formed, for example, by SUS (stainless).

The number of the pushers 18 installed is equal to that of chip regions to be brought into contact with a plurality of contact terminals which the below-described probe card has upon electrical testing of a semiconductor integrated circuit using the probe card of Embodiment 1. The elastomer 17 is formed, for example, by a silicone rubber and one elastomer is installed on each pusher 18. While having such an elastomer installed on the pusher, the pusher 18 is brought into contact with a predetermined position of the thin film probe 20 and applies a pushing pressure to the individual chip regions. By the application of this pushing pressure, deformation can be made according to the surface shape of a wafer to be tested, which will however be described later.

The receiving pin plate 13, POGO pin supporting plates 14,15, elastomer 17 and pusher 18 are integrated with high precision by being fixed to the retainer plate 19 by a screw 23.

The silicone rubber 22 is placed between the POGO pin supporting plate 15 and stretch holder 21. By application of a load in a height direction, a relative position between the POGO pin supporting plate 15 and stretch holder 21 in the XY direction is fixed.

Such a lower pushing unit is fixed by the adjust bolt 10 which was described based on FIG. 1 and integrated with the above-described upper pushing unit (refer to FIG. 1) and multilayer wiring substrate 1 (refer to FIG. 1).

FIG. 4 is a fragmentary cross-sectional view of the lower pushing unit.

As illustrated in FIG. 4, a protruding contact terminal 24 is formed over the lower surface (first surface) of the thin film probe 20. Over the upper surface (second surface) of the thin film probe 20, a land (second electrode) 25 is formed. The contact terminal 24 and land 25 are electrically connected via an interconnect 26 formed in the thin film probe 20. Under such a state, the tip of the POGO pin 12 has contact with the land 25, whereby the POGO pin 12 is electrically connected with the contact terminal 24. In the semiconductor prober of Embodiment 1, such a contact terminal 24 gets contact with an electrode (test pad) formed over the main surface of the chip region, whereby an electrical testing of a semiconductor integrated circuit device is carried out. Even when something wrong such as disconnection of the interconnect 26 happens in the thin film probe 20 and repairing of the probe card is needed as in the conventional case, only the replacement of the thin film probe 20 with a new one of the same kind is necessary so that time for repair can be reduced.

Over the upper surface of the thin film probe 20, a reinforcing material (first reinforcing member) 27 has been formed. As this reinforcing material 27, a material having a linear expansion coefficient (thermal expansion coefficient (first linear expansion coefficient)) substantially equal to that of a wafer to be tested is selected. This makes it

possible to keep the relative position between the contact terminal 24 and the electrode (test pad) formed over the main surface in the chip region uniformly even by a temperature change, if any, and moreover, to bring the contact terminal 24 into contact with a predetermined electrode (test pad) without failure. When a wafer to be tested is composed mainly of silicon, silicon and 42 alloy can be given as examples of the material of the reinforcing material 27.

Over the contact terminal 24, a groove 28 is formed in the reinforcing material 27 and an elastomer (first elastic material) 29 is formed to fill the groove 28 therewith so as to exceed the groove by a predetermined amount. Over the elastomer 29, the pusher 18 and elastomer 17 are disposed in such a manner that the pusher 18 is sandwiched between the elastomers 17 and 29. Thus the elastomer 29, pusher 18 and elastomer 17 constitute a pushing mechanism 30. In this Embodiment 1, a material softer (having a smaller elastic modulus) than the elastomer 17 is selected for the elastomer 29. According to the test made by the present inventors, by selecting a proper material for the elastomer 29, the contact terminal 24 can be brought into contact with the electrode (test pad) without failure even when strains such as warp appear in a wafer to be tested and a plurality of electrodes (test pads) with which the contact terminal 24 come in contact have not a uniform height. This makes it possible to improve the throughput of the electrical testing of a semiconductor

integrated circuit device using the probe card of Embodiment 1.

FIG. 5 is a plan view of the whole plane pattern of the thin film probe 20 illustrated while paying particular attention to the layout patterns of the land 25 and interconnect 26. It shows, for example, a constitution permitting simultaneous testing of 8 rows by 8 columns, 64 chip regions in total. FIG. 6 illustrates a part of the plane pattern of FIG. 5 and is a fragmentary enlarged plan view illustrating portions corresponding to two chip regions. In FIG. 6, only the tip portion of the contact terminal 24 is illustrated and per chip region, 26 contact terminals 24 are disposed.

In this Embodiment 1, any two adjacent lands 25 are separated by a space (first space) t1 wider than the space between the tip portions of any two adjacent contact terminals 24 and at the same time, these lands are equally spaced. This is because the position of the tip portion of the contact terminal 24 is determined by the position of an electrode (test pad) which is to be brought into contact with the contact terminal 24 and is formed over the main surface of a wafer to be tested, but the land 25 can be disposed to facilitate leading of the interconnect 26 and disposal of the POGO pin 12. In this Embodiment 1, the space t1 between any two adjacent lands 25 can be set, for example, at about 0.65 mm when the chip size is about 5 mm × 5 mm, 26 contact terminals 24 are disposed and the space between the tip

portions of any two adjacent contact terminals 24 is about several tens of μm.

According to the thin film probe 20 as described above, since the tip portion of the contact terminal 24 is disposed in alignment with each electrode (test pad) all over the main surface of a wafer to be tested to cause the POGO pin 12, which is to be electrically connected with the contact terminal 24, to extend vertically upwards, the chip size can be reduced and even if the electrodes (test pads) become small and arranged at a narrow pitch, wafer-level testing of a semiconductor integrated circuit can be made irrespective of the arrangement of the electrodes (test pads).

FIG. 7 is a plan view of the whole planar pattern of the thin film probe 20 illustrated while paying particular attention to the layout pattern of the land 25 and reinforcing material 27. Similar to FIG. 5, it shows, for example, a constitution permitting simultaneous testing of 8 rows by 8 columns, 64 chip regions in total. FIG. 8 illustrates a part of the planar pattern of FIG. 7 and is a fragmentary enlarged plan view illustrating portions corresponding to two chip regions. Similar to FIG. 6, in FIG. 8, only the tip portion of the contact terminal 24 is illustrated and per chip region, 26 contact terminals 24 are disposed. In FIG. 8, a region in which the reinforcing material 27 is formed is distinguished by hatching.

As illustrated in FIGS. 7 and 8, on the upper surface of

the thin film probe 20, a region in which a groove 28 is formed for embedding the elastomer 29 (refer to FIG. 4) therein, a region in which the land 25 is disposed and a region in which a groove for preventing a short circuit between a plurality of lands 25 is formed are disposed, while the reinforcing material 27 is formed in a region other than these three regions. As described above, the reinforcing material 27 is formed of a material having a linear expansion coefficient (thermal expansion coefficient) almost equal to that of a wafer to be tested so that by forming the reinforcing material 27 in a wide region on the upper surface of the thin film probe 20, it is possible, even if a temperature change occurs, to always keep constant the relative position between the contact terminal 24 and the electrode (test pad) formed over the main surface of the chip region.

In order to bring the contact terminal 24 (refer to FIG. 4) into contact with the electrode (test pad) in a chip region to get electrical conduction between the contact terminal 24 and the electrode (test pad), it is necessary to break a natural oxide film (not illustrated) formed over the surface of the electrode (test pad) to bring the contact terminal 24 into contact with the electrode (test pad). When the contact terminal 24 (refer to FIG. 4) of the probe card of Embodiment 1 is replaced with a probe card having a contact terminal made of a cantilever type probe needle, the natural oxide film is

broken by wiping of the contact terminal after the contact terminal and the electrode (test pad) are brought into contact. There is however a potential danger that by this wiping for breaking the natural oxide film, the surface of the electrode (test pad) itself may be damaged. Such a scratch on the surface of the electrode (test pad) presumably lowers the adhesive force between the electrode (test pad) and a bonding wire when the electrode (test pad) is connected with the bonding wire in the later step. In addition, the electrode (test pad) becomes smaller with a chip size reduction, which leads to a relative increase in a ratio of the scratched region in the surface of the electrode (test pad). This may presumably cause further lowering in the adhesion between the electrode (test pad) and bonding wire.

The contact terminal 24 of Embodiment 1 reaches the surface of the electrode (test pad) itself in such a manner that the tip portion of it pierces the natural oxide film under pushing pressure by the pushing mechanism 20 (refer to FIG. 4), whereby the electrical conduction between the contact terminal 24 and the electrode (test pad) is produced. Compared with the use of a contact terminal made of a cantilever type probe needle, the number of scratches formed on the surface of the electrode (test pad) itself can be reduced. In other words, it is possible to prevent the inconvenience such as lowering in adhesion between the electrode (test pad) and a bonding wire which will be connected in the later step.

In the next place, manufacturing steps of the thin film probe 20 which was described based on FIGS. 4 to 8 will next be described using FIGS. 9 to 16. FIGS. 9 to 16 are fragmentary cross-sectional views of the thin film probe 20 during the manufacturing step.

As illustrated in FIG. 9, on both sides of a wafer 41 made of silicon and having a thickness of from about 0.2 mm to 0.6 mm, a silicon oxide film of about 0.5 μm in thickness is formed by thermal oxidation. With a photoresist film as a mask, the silicon oxide film on the main surface side of the wafer 41 is etched to form an opening portion reaching the wafer 41 in the silicon oxide film on the main surface side of the wafer 41. With the remaining silicon oxide film as a mask, the wafer 41 is anisotropically etched with an aqueous solution of a strong alkali (for example, aqueous solution of potassium hydroxide), whereby a hole in the prismoid form surrounded by (111) plane is formed on the main surface of the wafer 41.

The silicon oxide film used as a mask upon formation of the hole 43 is then removed by wet etching with a mixture of hydrofluoric acid and ammonium fluoride. The wafer 41 is thermally oxidized to form a silicon oxide film 44 of about 0.5 μm in thickness all over the wafer 41 including the inside of the hole 43. A conductive film 45 is formed over the main surface of the wafer 41 including the inside of the hole 43. This conductive film 45 can be formed, for example, by depositing a chromium film of about 0.1 μm in thickness and a

copper film of about 1 μm in thickness successively by sputtering or deposition. Then, a photoresist film is formed over the conductive film 45. By photolithography, the photoresist film is removed from a region in which the contact terminal 24 (refer to FIG. 4) is to be formed in the later step to form an opening portion.

By electroplating with the conductive film 45 as an electrode, high-hardness conductive films 47,48,49 are deposited successively over the conductive film 45 which has appeared on the bottom of the opening portion of the photoresist film. In this Embodiment 1, a nickel film and a rhodium film can be given as examples of the conductive films 47,49 and conductive film 48, respectively. By the steps so far described, the contact terminal 24 can be formed from the conductive films 48,49. The conductive films 45,47 will be removed later, but the removing step will be described later.

After removal of the photoresist film, a polyimide film 50 is formed to cover the contact terminal 24 and conductive film 45. Then, an opening portion reaching the contact terminal 24 is formed in the polyimide film 50. This opening can be formed by boring using laser or dry etching with an aluminum film as a mask.

Over the polyimide film 50 including the inside of the opening, a conductive film 51 is formed. This conductive film 51 can be formed, for example, by depositing a chromium film of about 0.1 μm in thickness and a copper film of about 1 μm

in thickness successively by sputtering or deposition. After formation of a photoresist film over the conductive film 51, the resulting photoresist film is patterned by photolithography and an opening portion reaching the conductive film 51 is formed in the photoresist film. By plating, a conductive film 52 is formed over the conductive film 51 in the opening portion. In this Embodiment 1, a copper film or a laminate film obtained by successively depositing a copper film and a nickel film can be given as an example of the conductive film 52.

After removal of the photoresist film, with the conductive film 52 as a mask, the conductive film 51 is etched to form interconnects 26 made of the conductive films 51,52 and an alignment mark 53. The interconnect 26 can be electrically connected with the contact terminal 24 on the bottom of the opening portion.

Onto the main surface of the wafer 41, a polyimide adhesion sheet or epoxy adhesion sheet, for example, is attached to form an adhesive layer 54. A metal sheet 55 is then firmly adhered onto the upper surface of the adhesive layer 54. As a material of this metal sheet 55, that having a linear expansion coefficient which is low and at the same time, close to that of the wafer 41 must be selected. In this Embodiment, 42 Alloy (an alloy of 42% nickel and 58% iron and having a linear expansion coefficient of 4 ppm/°C) or Invar (an alloy of 36% nickel and 64% alloy and having a linear

expansion coefficient of 1.5 ppm/°C) can be given as an example of the material. Instead of the metal sheet 55, a silicon film having the same material quality with that of the wafer 41 may be formed, or a material having a linear expansion coefficient equal to that of silicon, for example, Super Invar (iron-nickel-cobalt alloy), Kovar (iron-nickel-cobalt alloy) or Cerasin (ceramic-resin mixture) may be employed. Such metal sheet 55 has, formed therein, an inspection hole 56 for visually confirming the alignment mark 53. This metal sheet 55 is firmly adhered to the adhesive layer, for example, by stacking the metal sheet 55, which has the inspection hole 56 formed therein, over the wafer 41 having the contact terminal 24 and alignment mark 53 formed thereon while aligning them by using the alignment mark 53 and inspection hole 53; and pressure bonding them under heat at the glass transition point of the adhesive layer 54 or greater while applying a pressure of about 10 to 200 kgf/cm^2 to them.

Firm adhesion of the metal sheet 55 by using the adhesive layer 54 makes it possible to improve the strength and increase the area of the thin film probe 20 thus formed. In addition, it becomes possible to prevent relative misalignment between the thin film probe 20 and a wafer to be tested, which will otherwise occur by the temperature upon test, thereby maintaining the relative positional accuracy between the thin film probe 20 and the wafer to be tested under various situations.

With a photoresist film 57 as a mask, the metal sheet 55 is etched. In Embodiment 1, this etching can be actualized by spray etching with an iron chloride solution.

After removal of the photoresist film 57, the adhesive layer 54 is perforated with the metal sheet 55 as a mask as illustrated in FIG. 10 to form an opening portion 58 reaching the interconnect 26. For this perforation, laser processing using an excimer laser or CO_2 gas laser, or dry etching can be employed. In the later step, the above-described land 25 (refer to FIG. 4) to be electrically connected with the interconnect 26 on the bottom of the opening portion 58 is formed in the opening portion 58.

As illustrated in FIG. 11, the metal sheet 55 is etched with a photoresist film 59 to form the reinforcing material 27 (including the groove 28) made of the metal sheet 55. The planar pattern of the reinforcing material 27 formed by this etching is the planar pattern of the reinforcing material 27 described based on FIGS. 7 and 8.

After removal of the photoresist film 59, the land 25 to be electrically connected with the interconnect 26 is formed in the opening 58 as illustrated in FIG. 12. This land 25 can be formed, for example, by successively stacking a copper film, a nickel film and a gold film one after another by electroplating with the interconnect 26 as an electrode. Since the land 25 is formed after formation of the reinforcing material 27 made of the metal sheet 55, the reinforcing

material 27 can serve as a ground layer, making it possible to prevent disorder of test signals upon testing step using the probe card of Embodiment 1.

As illustrated in FIG. 13, an elastomer 29 is formed in the groove 28. The elastomer 29 is formed so that a predetermined amount of it protrudes from the groove 28. In Embodiment 1, the elastomer 29 is formed, for example, by printing or applying, through a dispenser, an elastic resin in the groove 28, or placing a silicone sheet. As the elastomer 29, a material softer (having a smaller elastic modulus) than the elastomer 17 (refer to FIG. 4) must be selected as described above. This makes it possible to bring the contact terminal 24 into contact with a plurality of electrodes (test pads) without failure, even if strains such as warp are generated in the wafer to be tested and there appears a difference in the height among the electrodes (test pads) over the main surface of a wafer to be brought into contact with the contact terminal 24. In addition, the elastomer 29 changes partially and absorbs variations in the height of the tip of the individual contact terminals while relaxing an impact given when the tip of contact terminals 24 gets contact with the electrodes (test pads) arranged on the main surface of a wafer to be tested. It uniformly embeds itself, following the irregularities in the height of electrodes (test pads) and actualizes contact between the contact terminal 24 and electrode (test pad).

As illustrated in FIG. 14, the thin film probe frame 60 and process ring 61 are adhered to the reinforcing material 27 with an adhesive. Then, a protective film (not illustrated) is adhered to the thin film probe frame 60 and the process ring 61, while a ring-shaped protective film (not illustrated), that is, a film bored at the center thereof is adhered on the back side of the wafer 41. With these protective films as a mask, the silicon oxide film 44 is removed from the back side of the wafer 41 by etching with a mixture of hydrofluoric acid and ammonium fluoride.

After removal of the protective film, a fixing jig for silicon etching is attached to the wafer 41. This fixing jig for silicon etching is formed of an intermediate fixing plate 61, a stainless-made fixing jig 63, a stainless made lid 64, an O ring 65 and the like. This fixing jig for silicon etching is attached to the wafer 41 by screwing the thin film probe frame 60 down to the intermediate fixing plate 62, and loading the wafer 41 between the fixing jig 63 and lid 64 via the O ring 65. After the wafer 41 is equipped with the fixing jig for silicon etching, the wafer 41 which is a section material for the formation of the thin film probe 20 is removed by etching with an aqueous solution of a strong alkali (for example, an aqueous solution of potassium hydroxide).

Then, the silicon oxide film 44, conductive film 45 and conductive film 47 are removed successively by etching. Described specifically, the silicon oxide film 44 is etched

with a mixture of hydrofluoric acid and ammonium fluoride, a chromium film contained in the conductive film 45 is etched with an aqueous solution of potassium permanganate, and a copper film contained in the conductive film 45 and a nickel film serving as the conductive film 47 are etched with an alkaline copper etchant. By the steps so far described, a rhodium film which is a conductive film 48 (refer to FIG. 9) forming the contact terminal 24 appears from the surface of the contact terminal 24. The contact terminal 24 having the rhodium film formed on the surface thereof is able to have stabilized contact resistance, because solder and aluminum which are materials for the plurality of electrodes (test pads) on the main surface of the wafer to be brought into contact with the contact terminal 24 do not stick thereto easily, and the contact terminal has a higher hardness than nickel and is not oxidized easily.

After elimination of the fixing jig for silicon etching, a protective film 66 is adhered to the surface to which the thin film probe frame 60 and process ring 61 have been attached, and a protective film 67 is adhered onto the surface on which the contact terminal 24 is formed, as illustrated in FIG. 15. An anti-contamination material 68 is disposed in a region of the protective film 67 opposite to the contact terminal 24 in order to prevent the tip portion of the contact terminal 24 from contamination or breakage owing to the contact of it with the protective film 67. Then, the

protective film 66 over the alignment mark 53 is removed.

As illustrated in FIG. 16, an adhesive 69 is then applied between the thin film probe frame 60 and adhesive layer 54. An end portion of the thin film probe frame 60 is firmly adhered to the deformed adhesive layer 54 while pushing the thin film probe frame 60 downwards.

The protective films 66,67, and the polyimide film 50, adhesive layer 54 and adhesive 69 integrated along the peripheral portion of the thin film probe frame 60 are cut out, whereby the thin film probe 20 of Embodiment 1 is manufactured.

The manufacturing steps of the thin film probe 20 as described above are described also in Japanese Patent Application No. 2002-289377 filed by the present inventors.

For improving the throughput of a wafer-level test (for example, probe test) of a semiconductor integrated circuit, shortening of the time necessary for the test per wafer is requested. The time T0 required for the test per wafer is represented, for example, by the equation: $T0=(T1+T2)\times N+T3$, wherein T1 is time necessary for a single test by a semiconductor prober, T2 is time necessary for indexing of a probe card, N is the number of touchdown times to bring a probe (contact terminal 24 (refer to FIG. 4) in Embodiment 1) of a prober into contact with the wafer, and T3 is time necessary for replacement of the wafer to a new one. According to this equation, the number of touchdown times must be reduced in order to improve the throughput of a wafer-level

test of a semiconductor integrated circuit device. The shot efficiency K is represented by the following equation: $K=M1/(M2\times N)$, wherein M1 is the number of chip regions formed on one wafer and M2 is the number of chip regions with which a probe card can have contact simultaneously. The poor shot efficiency K means poor using efficiency of the probe card and an increase in the number of touchdown times. Also this equation for the determination of the shot efficiency K gives a suggestion about a decrease in the number of touchdown times.

Various examples of simultaneous testing of multiple chip regions (including simultaneous testing of super multiple chip regions) in the wafer-level test of a semiconductor integrated circuit and a shot efficiency of each example will next be described based on FIGS. 17 to 24.

FIG. 17 is a plan view illustrating one example of the layout of chip regions in a wafer plane which are to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 17, 312 chip regions are disposed within the plane of a wafer WH and each contact region (first region) CA with which a probe card can get in touch simultaneously is caused to correspond to 16 chip regions, that is, 2 chip regions in the lateral direction of the paper and 8 chip regions in the lengthwise direction so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed

by the contact of a probe card 13 times. In this case, the shot efficiency is about 78% when determined based on the above-described equation for determining the shot efficiency.

FIG. 18 is also a plan view illustrating one example of the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 18, 312 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card can get in touch simultaneously is caused to correspond to 24 chip regions in total, that is, 2 chip regions in the lateral direction of the paper and 12 chip regions in the lengthwise direction so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 18 times. In this case, the shot efficiency is about 72% when determined based on the above-described equation for determining the shot efficiency.

FIG. 19 is also a plan view illustrating one example of the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 19, 312 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card can get in

touch simultaneously is caused to correspond to 32 chip regions in total, that is, 4 chip regions in the lateral direction of the paper and 8 regions in the lengthwise direction so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 13 times. In this case, the shot efficiency is about 75% when determined based on the above-described equation for determining the shot efficiency.

FIG. 20 is also a plan view illustrating one example of the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 20, 312 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card can get in touch simultaneously is caused to correspond to 64 chip regions in total, that is, 8 chip regions in the lateral direction of the paper and 8 regions in the lengthwise direction so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 8 times. In this case, the shot efficiency is about 61% when determined based on the above-described equation for determining the shot efficiency.

FIG. 21 is also a plan view illustrating one example of

the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 21, 312 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card can get in touch simultaneously is caused to correspond to 100 chip regions in total, that is, 10 chip regions in the lateral direction of the paper and 10 regions in the lengthwise direction so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 4 times. In this case, the shot efficiency is about 78% when determined based on the above-described equation for determining the shot efficiency.

FIG. 22 is also a plan view illustrating one example of the arrangement, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 22, 312 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card (contact terminal 24) can get in touch simultaneously is caused to correspond to every other chip regions so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the

contact of a probe card twice. In this case, the number of chip regions with which the probe card can get in touch simultaneously is 168, The shot efficiency is therefore about 93% when determined based on the above-described equation for determining the shot efficiency.

FIG. 23 is also a plan view illustrating one example of the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 23, 856 chip regions are disposed within the plane of a wafer WH and each contact region CA with which a probe card (contact terminal 24) can get in touch simultaneously is caused to correspond to every four chip regions so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 4 times. In this case, the number of chip regions with which a probe card can get in touch simultaneously is 230. The shot efficiency is therefore about 93% when determined based on the above-described equation for determining the shot efficiency.

FIG. 24 is also a plan view illustrating one example of the layout, within a wafer plane, of chip regions to be tested by a semiconductor prober by single contact of a probe card. The chip regions are distinguished by hatching.

According to the example illustrated in FIG. 24, 828

chip regions are disposed within the plane of a wafer WH and a contact region CA with which a probe card (contact terminal 24) can get in touch simultaneously is caused to correspond to predetermined chip regions selected at equal intervals so that a test of a semiconductor integrated circuit for all the chip regions within the plane of the wafer WH can be completed by the contact of a probe card 8 times. In this case, the number of chip regions with which a probe card can get in touch simultaneously is 118. The shot efficiency is therefore about 88% when determined based on the above-described equation for determining the shot efficiency.

As described based on FIGS. 17 to 24, when the contact region CA is defined as a rectangular shape as illustrated in FIGS. 17 to 21, the shot efficiency becomes less than 80%, while it can be increased to 80% or greater when the contact region CA is defined by selecting chip regions of predetermined columns or rows or selecting them at some intervals from the whole wafer WH plane as illustrated in FIGS. 22 to 24. With regards to the touchdown times, a drastic reduction can be realized in the cases shown in FIGS. 22 to 24, compared with the case where the contact region CA has a rectangular shape (except the examples shown in FIGS. 20 and 21). In other words, the time necessary for the test of one wafer can be reduced by defining the contact region CA by selecting chip regions of predetermined columns or rows, or selecting them at some intervals from the whole wafer WH plane

as illustrated in FIGS. 22 to 24. As a result, the throughput of the wafer-level test of a semiconductor integrated circuit can be improved.

When the probe needle is a cantilever type, there is a potential danger that the pitch between electrodes (test pads) within a chip region decreases with narrowing thereof, leading to difficulty in insertion of probe needles to the probe card. When the probe needle is a cantilever type and the electrodes (test pads) formed in the chip region are drawn up in two lines along two sides opposite each other, insertion of pins is possible in the case of the contact region CA corresponding to dual row chip regions as illustrated in FIGS. 17 and 18. When the contact region includes more chip regions (for example, as illustrated in FIGS. 19 to 21) or when a contact region CA corresponds to chip regions of predetermined rows or columns or chip regions selected at some intervals in the whole wafer WH plane (for example, as illustrated in FIGS. 22 to 24), it becomes impossible to insert the pins in consideration of the extending direction of the probe needles. In other words, for a cantilever type probe needle, simultaneous testing of multiple chip regions as illustrated in FIGS. 22 to 24 which can actualize a high shot efficiency and less touchdown frequency is impossible. On the other hand, in the probe card of Embodiment 1 which was described based on FIGS. 1 to 16, simultaneous testing of multiple chip regions as illustrated in FIGS. 22 to 24 can be carried out because

the tip portion of the contact terminal 24 (refer to FIG. 4) can be aligned with the electrode (test pad) all over the main surface of a wafer WH to be tested. It is also possible to decrease the number of touchdown times to once when the tip portion of the contact terminal 24 is disposed in alignment with the each of the electrodes (test pads) in all the chip regions formed in a wafer WH to be tested.

Based on FIG. 25, one example of the fabrication method of the semiconductor integrated circuit device of Embodiment 1 will next be described. FIG. 25 is a flow chart illustrating the fabrication method of the semiconductor integrated circuit device. In this Embodiment 1, MCP (Multi Chip Package) having both SRAM (Static Random Access Memory) and Electric Erasable Programmable Read Only Memory EEPROM (which will hereinafter be called "flash memory") is employed as one example of the semiconductor integrated circuit device.

By a pretreatment step, many elements constituting SRAM and flash memory are formed over the device surface (main surface) of two wafers, respectively. Described specifically, by this step, each desired integrated circuit is formed over a semiconductor wafer made of, for example, single crystal silicon by repeating, in accordance with the respective specifications of the SRAM and flash memory, wafer processing steps such as oxidation, diffusion, impurity implantation, formation of wiring patterns, formation of an insulating layer and formation of a wiring layer (Steps SS1, SF1).

Then, DC operating characteristic test of an MIS constituting TEG (Test Element Group) formed in a scribe region for dividing the wafer into a plurality of chip regions is performed. Described specifically, a threshold voltage of the MISs forming SRAM and flash memory is inspected by measuring the threshold voltage of the MIS constituting TEG (Steps SS2, SF2).

The wafer having many elements formed thereover is then tested (wafer level test) (Steps SS3, SF3). A burn-in test and a probe test are carried out successively here. Prior to the burn-in test, a simple probe test is sometimes inserted as needed. In the burn-in test, at least a rated supply voltage is applied to the wafer in a high temperature (for example, 125 to 150°C) atmosphere to pass an electric current through an integrated circuit. By application of such temperature and voltage stresses to chips, chips which may be defective in future are screened. In the probe test, on the other hand, a function test in which the memory function of the wafer is tested using a specific test pattern according to the reading and writing operations to SRAM and flash memory in a high temperature (for example, 85 to 95°C) atmosphere to confirm whether the wafer functions to specification or not; open/short test between input and output terminals; leakage current inspection; DC test such as measurement of supply current; AC test for testing AC timing of memory control and the like are conducted. In this wafer-level probe test step, a

semiconductor prober having the probe card of Embodiment 1 as described in FIGS. 1 to 16 is employed. The probe card of Embodiment 1 can also be used in the wafer-level burn-in test step. Such a wafer-level test makes it possible to feed back the data of the burn-in test on defective wafers and the like to the pretreatment step, by which the inconvenience in the pretreatment step can be avoided.

In the steps SS3, SF3 as described above, a test such as long-cycle test or refresh test (about 1 hour to several tens hours) having testing hour as long as that of burn-in test (about 8 to 48 hours) may be performed. Compared with the test performed after division into individual chips, such a test conducted in the wafer form while spending long hours enables to drastically improve the through-put of the fabrication of the semiconductor integrated circuit device of Embodiment 1.

Elements which have been found defective by the burn-in test and probe test are then repaired by exposing them to a laser light. Described specifically, in this step, failed bits of SRAM and flash memory are found by analyzing the results of the probe test and fuse of the redundant repair bits corresponding to the failed bits is cut by the laser light or by cutting an electric fuse via the input of external voltage, whereby they are repaired by redundant repair treatment (Steps SS4, SF4). This repair step may be followed by a wafer-level burn-in test step and wafer-level probe test step similar to those described in the steps SS3, SF3. These steps are for

confirming the completion of the replacement of the failed bits with redundant repair bits by the redundant repair treatment. Interference test, for example, disturb refresh test of a memory cell of SRAM and flash memory which can be carried out only after the redundant repair treatment may be performed. The memory cell of the flash memory may be subjected to wafer-level write/erase test (Steps SS5, SF5).

The wafer having SRAM formed thereover and another wafer having flash memory formed thereover are each cut into chips (Steps SS6, SF6). Non-defective wafer may be shipped as a product without cutting into chips (Steps SS7, SF7).

Steps necessary for the fabrication of the respective chips having SRAM and flash memory formed thereover into MCP include a die bonding step for loading these chips over a package substrate, a wire bonding step for electrically connecting the pad of each chip with a pad over the package substrate via a wire, a resin molding step for molding the chip and wire portions with a resin in order to protect them, and a lead forming step for forming and surface treating an outer lead. The wire bonding can be replaced with flip chip bonding (Step SP7). The MCP thus fabricated can be shipped as a product and provided for users (Step SP8).

According to the fabrication method of the semiconductor integrated circuit device of Embodiment 1, the burn-in test and probe test are performed prior to the fabrication of MCP so that defective chips discovered by the burn-in test or

probe test can be repaired. It is therefore possible to fabricate the MCP by KGD, leading to a great improvement in the yield of MCP. With an increase in the number of chips loaded on the MCP, the improving effect becomes greater.

By performing the burn-in test and probe test in the wafer form, the total index time can be shortened. In addition, by the wafer level test, the number of chips to be tested simultaneously can be increased. These advantages enable to improve the throughput of the wafer testing step, leading to a reduction in the fabrication cost of the semiconductor integrated circuit device of Embodiment 1.

(Embodiment 2)

FIG. 26 is a perspective view illustrating the constitution of a lower pushing unit of Embodiment 2 to be attached to the lower surface of the multilayer wiring substrate 1 (refer to FIG. 1) as described in Embodiment 1.

The lower pushing unit of Embodiment 2 is substantially similar to that of Embodiment 1 except for the constitution (refer to FIG. 3) of the lower pushing unit and pusher 18 (refer to FIG. 3). As illustrated in FIG. 26, the pusher 18 is replaced with a pusher (pushing member) 18A in the lower pushing unit of Embodiment 2. The pusher 18 of Embodiment 1 applies a pushing pressure to each chip region by being disposed in the number equal to the number of chip regions which the probe card gets in touch simultaneously. With regards to the pusher 18A in Embodiment 2, one pusher 18A

applies a pushing pressure to a plurality of chip regions, because the number of the pushers 18A of Embodiment 2 is smaller than that of the chip regions with which the probe card gets in touch simultaneously. For example, when the chip regions with which the probe cans get in touch simultaneously are arranged in 8 rows and 8 columns, one pusher 18A applies a pushing pressure to chip regions of one row or one column, that is, 8 chip regions.

In Embodiment 2, similar effects to those of Embodiment 1 are available.

(Embodiment 3)

FIG. 27 is a fragmentary cross-sectional view of a lower pushing unit of Embodiment 3 to be attached to the lower surface of the multilayer wiring substrate 1 (refer to FIG. 1) as described in Embodiment 1.

The lower pushing unit of Embodiment 3 is substantially similar to that of Embodiment 1 except for the constitution of a thin film probe 20 which the lower pushing unit has. As illustrated in FIG. 27, the thin film probe 20 of Embodiment 3 is formed so as to flatten the surface of the land 25 of the thin film probe 20 (refer to FIG. 4) of Embodiment 1. In other words, the surface of the land 25 with which the POGO pin 12 is in contact is planarized by increasing the thickness of each of a copper film 25A, a nickel film 25B and a gold film 25C constituting the land 25.

By flattening the surface of the land 25, it is possible

to prevent the inconvenience such as widening of indentations formed in electrodes (test pads) which will otherwise occur as follows: the impact upon contact of the contact terminal 24 with a wafer (electrode (test pad) formed over the main surface of a chip region) to be tested causes the slide of the POGO pin 12 and land 25; and an impact caused by this slide of the POGO pin 12 and land 2 is transmitted to the contact terminal 24 and widens indentations which have been formed in the electrode (test pad) by the contact of the contact terminal 24. By preventing such widening of indentations, it becomes possible to definitely prevent lowering in adhesive force between the electrode (test pad) and a bonding wire when the bonding wire is connected to the electrode (test pad) in the later step.

In the constitution (refer to FIG. 4) of the land 25 of Embodiment 1, similar effects are available by applying, to the POGO pin 12 in advance, a preload capable of pushing the land 25 by its predetermined pushing pressure.

In Embodiment 3 as described above, similar effects to those of Embodiments 1 and 2 are available.

The present invention was described specifically based on some embodiments. It should however be borne in mind that the present invention is not limited to or by them. It is needless to say that the invention can be modified within an extent not departing from the scope of the invention.

For example, in the above-described embodiments, a wafer

made of silicon which has been anisotropically etched is used as a section material for the formation of a thin film probe. The material is not limited to silicon and in addition, treatment other than anisotropic etching may be adopted. For example, glass which has been dry etched can be used instead.

In the above-described embodiments, a hole of prismoid in form is made by anisotropically etching a wafer which will serve as a section material for the formation of a thin film probe. The hole may be pyramid in form instead of prismoid. The hole can be used insofar as it permits the formation of a contact terminal which can maintain stable contact resistance at a small needle pressure.

An advantage available by the typical inventions, of the inventions disclosed by the present application, will next be described briefly.

By the present invention, the throughput of wafer-level electrical testing of a semiconductor integrated circuit device can be improved.